3.3 kV 4H-SiC Planar-Gate MOSFETs Manufactured using Gen-5 PRESiCE™ Technology in a 4-inch Wafer Commercial Foundry

Aditi Agarwal, B. Jayant Baliga
Department of Electrical and Computer Engineering
North Carolina State University
Raleigh, NC 27606, USA
Email: aagarw12@ncsu.edu

Michel M.A. Francois, Ed Maxwell, Nathaniel Berliner, Marc Papageorge
SiCamore Semi
Bend, OR 97702, USA
Email: MFrancois@sicamoresemi.com

***Abstract*—The successful fabrication of 3.3 kV 4H-SiC Planar-Gate MOSFETs in a 4" commercial foundry using the Gen-5 PRESiCE™ technology is reported in this paper. Both Accumulation-channel MOSFETs (ACCUFETs) and Inversion-channel MOSFETs (INVFETs) were successfully manufactured. The electrical characteristics of the two types of fabricated devices are compared in this paper. The wafer yield data indicates that gate-source shorts were the yield-limiting criteria. This effort establishes a second source foundry for manufacturing SiC power devices in the United States.**

Keywords—4H-SiC, Wide Band Gap Semiconductor Device Fabrication, Foundry, Power MOSFET, ACCUFET, INVFET

I. Introduction

Silicon carbide (4H-SiC) power Metal-Oxide-Semiconductor-Field-effect-Transistors (MOSFETs) have been recently commercialized due to their superior performance compared with Silicon (Si) Insulated-Gate-Bipolar-Transistors (IGBTs). These devices are widely used in power electronic circuits for applications such as motor drives for electric vehicles and industrial applications [1]. Many commercial semiconductor companies utilize in-house manufacturing capability. It is preferable to utilize a foundry for manufacturing the SiC devices to create a high volume production capability to drive down cost. One 6-inch wafer 4H-SiC power device manufacturing foundry was established in the United States in 2015 by PowerAmerica. The NCSU engineered Gen-1 and Gen-3 PRESiCE™ technology was created and licensed to encourage greater participation in SiC power device production [2]. The Gen numbers refer to the budget period in which the technology development was sponsored by the PowerAmerica Institute. However, there is a need for a second source foundry to complement the manufacturing of SiC power devices by many fabless device vendors. This paper reports the successful establishment of a NCSU engineered Gen-5 PRESiCE™ technology at the SiCamore Semi 4-inch 4H-SiC wafer foundry at Bend, OR.

SiC power MOSFETs with 600 V, 1.2 kV and 2.3 kV voltage ratings have been previously manufactured using the Gen-3 PRESiCE™ technology [3,4,5]. It has been demonstrated that 1.2 kV accumulation-channel MOSFETs (ACCUFETs) exhibit better on-state and switching characteristics compared to inversion-channel MOSFETs (INVFETs) [6]. In this paper, the successful manufacturing of SiC power MOSFETs with a higher voltage rating of 3.3 kV at a 4 inch 4H-SiC foundry is described. The electrical characteristics of the ACCUFETs and INVFETs with 3.3 kV rating are compared for the first time.

II. Device Structure and Fabrication

A. Device Structure

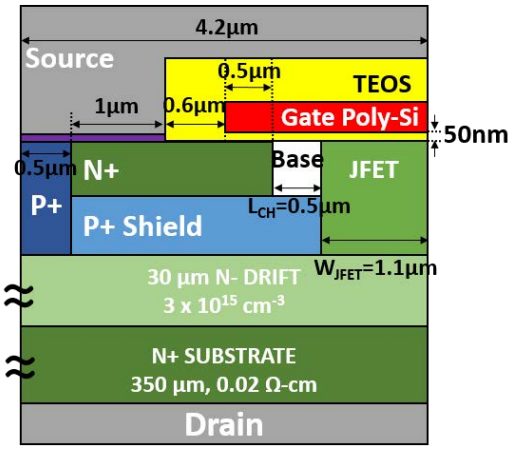

Fig. 1 Cross-section of the fabricated 3.3 kV 4H-SiC Accumulation and Inversion-channel MOSFETs.

Fig. 1 shows the structure with dimensions for the SiC power MOSFET devices manufactured in this work. The MOSFETs have a cell pitch of 4.2 µm and were fabricated with a linear cell topology [3]. Both the ACCUFET and INVFET had a gate oxide thickness of 50 nm with an active area of 0.045 cm^2.The same device design was used for the ACCUFETs and INVFETs in this paper for comparison of relative performance. The hybrid-JTE edge termination was used to achieve the 3.3 kV blocking voltage capability [7].

The devices were fabricated using epitaxial layers with thickness of 30 µm and N-type doping of 3×10^{15} cm^{-3} grown on 350 µm N^+ substrates with 0.02 Ω-cm resistivity to obtain a breakdown capability of 3.3 kV. The doping profiles for the N^+,

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P+, P-Base and JFET regions are shown in Fig. 2 along a horizontal line just below the gate oxide. The doping profile along the vertical direction is shown in Fig. 3 for all the different regions. Two different types of base ion implantation profiles were used on different wafers to create the accumulation and inversion channels as shown in Fig. 3.

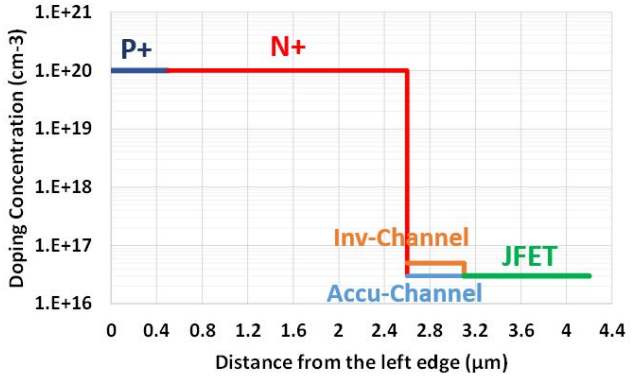


Fig. 2 Doping profile along a horizontal line through SiC below the gate oxide.

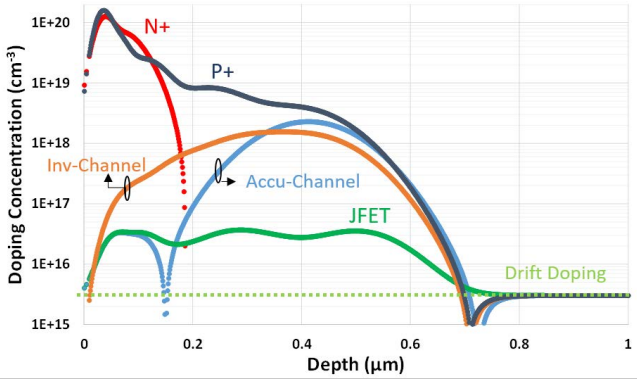


Fig. 3 Doping profile in the vertical direction through the P+, N+, JFET, the accumulation-channel, and inversion channel base regions.

B. Device Fabrication

The 3.3 kV 4H-SiC power MOSFET fabrication was performed at the 4-inch SiCamore Semi foundry, Bend, OR, using the Gen-5 PRECiSE™ process developed by North Carolina State University. Nitrogen ion implantation was carried out over the entire active area to enhance the doping level to 3×10^{16} cm^{-3} for the JFET region. The N^+ and P^+ regions had a high doping concentration of 1×10^{20} cm^{-3} to form a good ohmic contact. The P^+ shield and channel regions were formed simultaneously with a single Al P-type implant. For the accumulation-channel devices, a peak P^+ shield region concentration of 3×10^{18} cm^{-3} and an N-type channel concentration of 3×10^{16} cm^{-3} was obtained. For the inversion-channel devices, a peak P^+ shield region concentration of 2×10^{18} cm^{-3} and P-type channel concentration of 5×10^{16} cm^{-3} was obtained. The ion implant activation anneal was carried out at 1675 ºC for 30 minutes with a carbon cap to enable dopant activation and lattice recovery.

Oxidation was done at 1100 ºC to form a 20 nm thick sacrificial oxide followed by its removal to reduce the surface roughening and damage caused by ion implantation. Thereafter, gate oxidation was done at 1175 ºC to form the 50 nm gate oxide with 2 hours of NO annealing for surface passivation and improving channel mobility. This was followed by deposition of 5000 Å phosphorus-doped polysilicon and gate patterning. 5000 Å of inter-layer dielectric (TEOS) was then deposited and patterned to form the Ohmic contact window. 1000 Å Ni was deposited on the front side and 1500 Å on the back side of the wafer and rapid thermal annealing was carried out at 900 ºC for 2 minutes to form the source and drain Ohmic contacts. The oxide at the cell edges was then patterned to expose the gate poly-Si pad. The top metal stack (Ti/TiW/AlCu) was deposited and patterned to form the source, drain and gate contacts. An oxynitride passivation layer was then deposited and patterned.

III. Device Characteristics and Discussion

Extensive wafer-level measurements were performed on the fabricated wafers using the Semi-Automatic Signatone probe station with the B1505 Keysight curve tracer. The measurements included: (a) Output characteristics, (b) Transfer characteristics, (c) Blocking and leakage current characteristics, (d) 3rd quadrant characteristics, and (e) Input, output and reverse transfer characteristics. The measured values for the 3.3 kV ACCUFETs and INVFETs are compared in this section.

A. Output Characteristics

Fig. 4 shows the output characteristics for the fabricated 3.3kV ACCUFET (blue) and INVFET (orange) at various gate bias voltages ranging from V_{gs}=0 to 20 V in 5 V steps. The ACCUFET exhibits a lower on-resistance and larger transconductance compared to the INVFET due to the higher channel mobility and lower threshold voltage for the accumulation-channel [4]. The values of the specific on-resistance ($R_{on,sp}$) measured at V_{gs}=20 V and I_d=1 A are 13.8 and 19.8 mΩ-cm^2 for the ACCUFET and INVFET, respectively. The transconductance for the ACCUFET is 15 % larger than for the INVFET due to the larger accumulation channel mobility compared with inversion channel mobility.

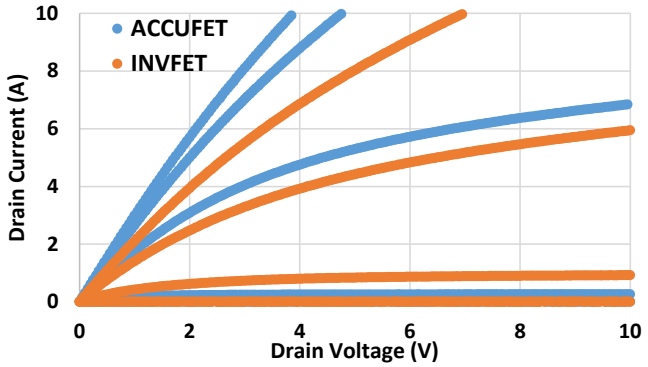


Fig. 4 Output characteristics for the fabricated 3.3 kV ACCUFET and INVFET devices using V_{gs}=0 to 20 V in 5 V steps.

B. Transfer Characteristics

Fig. 5 shows the measured transfer characteristics for the fabricated 3.3 kV ACCUFET and INVFET devices at a drain bias of 0.1 V. The threshold voltage (V_{th}), measured at drain current, I_d= 1 mA was 2.7 and 4.9 V for the ACCUFET and INVFET devices respectively. The threshold voltage is expected

to be lower for ACCUFET devices compared with the INVFET devices as explained in previous publications [8].

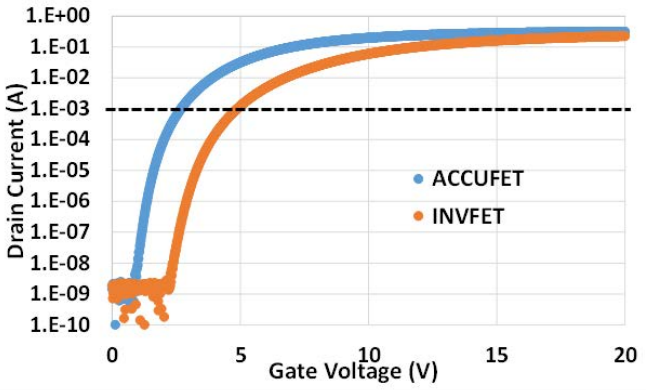


Fig. 5 Transfer characteristics for the fabricated 3.3 kV ACCUFET and INVFET devices at V_{ds}=0.1 V.

C. 3rd Quadrant Characteristics

Fig. 6 shows the measured 3rd quadrant characteristics for the fabricated 3.3 kV ACCUFET and INVFET devices. The voltage drop in the 3rd quadrant at a current of 2.25 A (50 A/cm^2) for the INVFET is 4.7 V while that for the ACCUFET is 3.6 V. This is expected behavior due to higher channel potential for the INVFET devices as previously studied in detail [9].

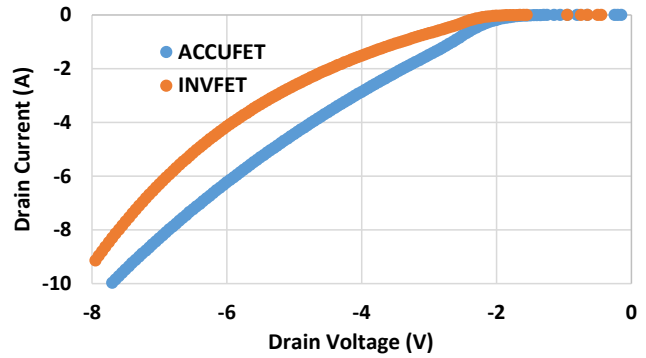


Fig. 6 3rd quadrant characteristics for the fabricated 3.3 kV ACCUFET and INVFET devices at V_{gs}=0 V.

D. Reverse Blocking Characteristics

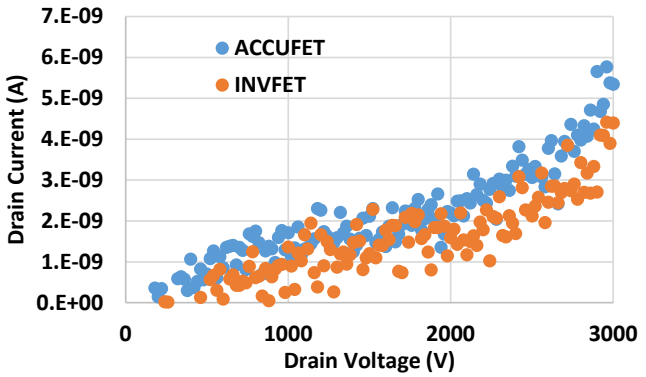


Fig. 7 Blocking characteristics for the fabricated 3.3 kV ACCUFET and INVFET devices at V_{gs}=0 V.

Fig. 7 shows a plot of leakage current versus drain voltage in the off-state up to 3 kV using V_{gs}= 0 V. Very low leakage current < 10 nA was observed at 3 kV for both devices indicating that the hybrid JTE edge termination offers robust protection against breakdown at the edges. It also demonstrates that the channel potential barrier for the ACCUFET device is sufficient to prevent reach-through breakdown [8].

E. Input, Output and Reverse Transfer Capacitances

The measured input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances are shown in Fig. 8. These capacitance values are helpful in determining the switching performance of power devices. The measured C_{iss}, C_{oss} and C_{rss} values are close for both devices due to the same basic cell structure shown in Fig. 1. The values for C_{oss} and C_{rss} decrease with drain bias due to expansion of the depletion layer [8].

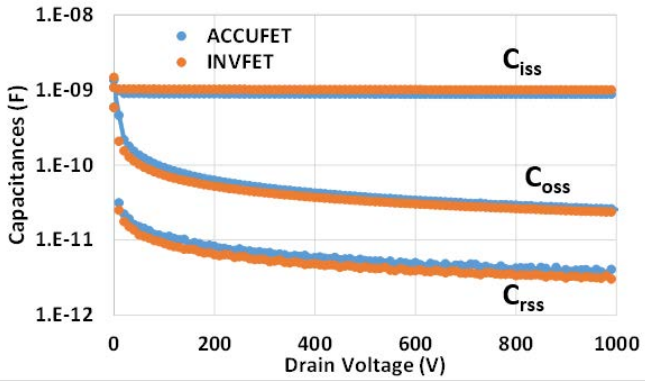


Fig. 8 Measured input, output and reverse transfer characteristics for the fabricated 3.3 kV ACCUFET and INVFET devices up to V_{ds} of 1 kV.

IV. Wafer Yield

An image of the completed 4" wafer, fabricated at SiCamore Semi with the NCSU chip designs, is shown in Fig. 9. Fig. 10 shows the $R_{on,sp}$ wafer-map for accumulation-channel wafer (a) and inversion-channel wafer (b). The $R_{on,sp}$ is reported at the drain current of 1 A and gate voltage of 20 V. The grey boxes represent gate-source shorts.

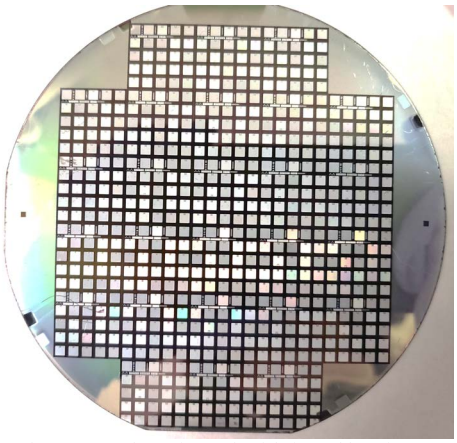
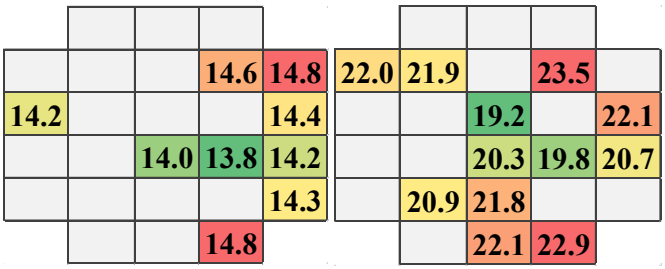


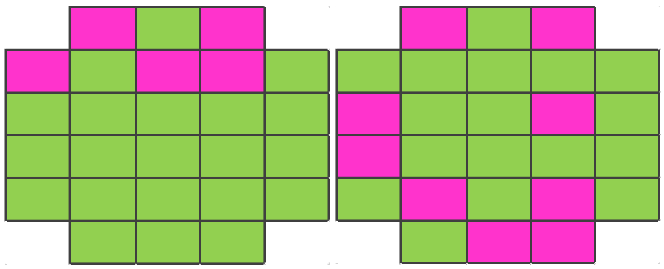
Fig. 9 Picture of a processed 4" SiC wafer fabricated by SiCamore Semi with NCSU designed 3.3 kV MOSFET devices.



(a) (b)

Fig. 10 Specific on-resistance wafer-map (at V_{gs}= 20 V, I_d= 1 A) for (a) Accumulation-channel wafer, and (b) Inversion-channel wafer. Grey boxes indicate gate-source shorts.

Fig. 11 shows the breakdown voltage wafer-map for the accumulation-channel wafer (a) and the inversion-channel wafer (b). The green boxes represent dies with breakdown voltage greater than 3 kV and pink boxes represent dies with lower breakdown voltages.



(a) (b)

Fig. 11 Wafer-map for breakdown voltage for (a) Accumulation-channel wafer and (b) Inversion-channel wafer. Green boxes indicate dies with breakdown voltage > 3 kV and pink boxes indicate dies with lower breakdown voltage.

From the $R_{on,sp}$ and breakdown voltage wafer-maps, it can be concluded that gate-source shorts are the yield-limiting factor. The high breakdown voltages for most dies indicates accurate epitaxial layer parameters for the hybrid JTE edge termination.

TABLE I
EXPERIMENTAL RESULTS

Characteristics	ACCUFET	INVFET
*Avg. $R_{on,sp}$ [mΩ-cm^2]	13.8	19.8
V_{th} (@ 1mA) [V]	2.7	4.9
3rd Quad V_f (@ 2.25A) [V]	3.6	4.7
C_{iss} (@ V_d=1 kV) [pF]	872	998
C_{oss} (@V_d=1 kV) [pF]	25.5	23.3
C_{rss} (@ V_d=1 kV) [pF]	3.6	3.0
$C_{iss,sp}$ (@ V_d=1 kV) [nF/cm^2]	19.4	22.2
$C_{oss,sp}$ (@V_d=1 kV) [nF/cm^2]	0.6	0.5
$C_{rss,sp}$ (@ V_d=1 kV) [pF/cm^2]	80	67
HF-FOM (R_{on}*C_{rss}) [mΩ-pF]	1104	1327
FOM (C_{iss}/C_{rss})	242	333

*$R_{on,sp}$ @V_{gs}=20V, I_d=1A, includes $R_{sub,sp}$ (~0.7 mΩ-cm^2)

V. CONCLUSIONS

A summary of experimental results is given in Table I. It can be concluded that the specific on-resistance can be reduced by a factor of 1.4-times by using the ACCUFET structure when compared with the INVFET structure for a device with blocking voltage of 3.3 kV. The specific on-resistance for the devices is 3-times the ideal value consistent with state-of-the-art technology. The measured capacitances for both devices were similar due to the same device structure. The high frequency performance of SiC power MOSFETs can be compared by using the HF-FOM(R_{on}*C_{rss}). The HF-FOM(R_{on}*C_{rss}) for ACCUFET was found to be 1.2-times better than for the INVFET.

From the wafer-maps, the overall yield for the ACCUFETs and INVFETs was 34%. This yield was obtained after running only 2 lots of wafers. It will be increased in the future by running multiple lots while refining the processes.

In conclusion, the NCSU engineered Gen-5 PRESiCE™ technology was used to establish a SiC power MOSFET manufacturing capability at a 4-inch wafer foundry operated by SiCamore Semi with device performance for 3.3 kV rated devices consistent with state-of-the-art technology. This foundry can serve as a second source capability by fabless companies for manufacturing SiC power devices.

ACKNOWLEDGMENT

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